DETAILED ACTION

Response to Arguments

1. The cancellation of claim 19 effectively overcomes the 35 USC § 112, indefiniteness, rejection of the claim.

2. The amendments to claims 17 and 23 effectively overcome the objections to the claims.

3. Applicant's arguments filed 10/8/2009 regarding the art rejections of the claims have been fully considered but they are not persuasive. Although the amendments filed further limit the claims, the combination cited in the rejections in the previous office action assumed the further limitations and examiner considers the grounds of rejection to be the same.

The arguments against Pae on pages 8-11 are arguments against the reference in isolation but do not address its use in the combination. The arguments against Pae in the first paragraph of page 12 start off with a straw-man characterization of examiner's arguments regarding a single control voltage driving several transistors. As extensively laid out, examiner found that Pae teaches or reasonably suggests connecting a single Vramp in parallel to multiple instances of the S&H circuit each of which is connected to a data line. Examiner believes that this teaching is implicit within Pae but offered extensive reasoning for this belief because it was so obviously a feature of the circuit when applied to

a multiple column display that Pae never mentions it explicitly. The rest of the arguments in the paragraph are again arguments against Pae in isolation and in fact seem to simply cover the items that examiner, in the paragraph beginning at the end of page 6 of the previous office action, mentions that Pae does not explicitly disclose.

The arguments against Kimura in the last paragraph of page 12 and the firs paragraph of page 13 are arguments against the reference individually but fail to address the specific teachings applied in the combination.

In the second paragraph of page 13 applicant makes a conclusory statement about how different two circuits are but again fails to address the way that this particular point was covered in the rejections. The gist of this coverage being that Pae provides a voltage at least temporarily, to use a phrase from applicant's arguments not found in the claims, in parallel to the control terminal of a plurality of first current control means and the combination goes on to describe the use of a transistor in a configuration that generates a voltage based on the current flowing through the transistor and the reasons for such use.

The remaining paragraphs starting from the last paragraph of page 13 argue that Pae and Kimura are too operationally different to combine and thus that their combination would have been obvious only in light of improper hindsight. But it is not bodily incorporation that is required. Examiner pointed out the particular teachings drawn from each reference and the way and reasons

they were combined. That applicant can describe an alternate combination and reasoning does not address the combination as described.

Regarding the programming of a current source transistor within each pixel, applicant is correct that Pae places less of the disclosed circuitry within each pixel and Kimura places more of the circuitry within each pixel and the question is whether or not the partitioning of the circuitry involves an inventive step. Examiner has laid out the case for obviousness in detail and would be most persuaded by arguments that address the combination and arguments as presented; and also points out that, while applicant's arguments are centered on the partitioning of the circuitry of the current mirrors, the claims themselves do not require the argued partitioning.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 17-20, 22-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,917,350 to *Pae et al.* ("*Pae*") in view of U.S. Patent No. 7,138,967 to *Kimura* ("*Kimura*").

As to **claim 17**, *Pae* discloses a light emitting display including a multiplicity of elements arranged in rows and columns (see for example

Abstract), wherein the elements include a light-emitting means which emits light when a current flows through the light-emitting means (see for example Fig. 2 item "OEL"), a first current control means which is connected in series with the light-emitting means (see for example Fig. 2 item "P0") and, a first (see for example Fig. 3 item 23 "S&H circuit", refer to Fig. 4 to note that item 23 first connects its "ramp" terminal to its "Vramp" terminal and then switches to isolate "ramp" from further changes in "Vramp") and second (see for example Fig. 2 item "P1") switching means which are controlled by a respective first (see for example Fig. 3 the output of comparator 22) and second (see for example Fig. 2 item "SEL") switching signal and which are arranged between a control signal line and a control electrode of the first current control means (this can be seen by starting at "Vramp" in Fig. 3 and following the signal through the first switch "S&H circuit" to "ramp" through the second switch "P1" to the gate of the first current control means "P0"), wherein the control signal line (see for example Fig. 3 the connection from "Vramp" to "S&H circuit") is connected to one end of the series connection of the first and second switching means (this can be seen by starting at "Vramp" in Fig. 3 and following the signal through the first switch "S&H circuit" to "ramp" through the second switch "P1" to the gate of the first current control means "P0") of a multiplicity of elements (as noted in the abstract, the disclosure concerns an active matrix device; although the figures and description relate to a single pixel or sub-pixel the figures and description would fairly suggest to one of ordinary skill in the art the repetition of element over rows and/or columns; for

example the elements of Fig. 2 repeated for the intersections of all rows and columns resulting in multiple instances of P1 connected to the same data line; duplication at least for every row of at least the elements enclosed by the dashed line in Fig. 3 is implied by the connection of the "ramp" signal to the data line in Fig. 3 and the fact that the circuit doesn't really work for addressing unless the elements of Fig. 3 are duplicated at least for every simultaneously active data line; in describing this case of multiple connections to a single voltage source the specification refers to the signal on the data line as an "externally applied control voltage", see for example 4:27; the same nomenclature is used when describing the relationship of "Vramp" to the "S&H circuit" – see for example 5:3-5, "To the sample & hold circuit 23, an external ramp voltage is applied.", thus implying multiple instances of at least the "S&H circuit" supplied by a common "Vramp";).

Although examiner feels that the above citations show that "Vramp" was taught to connect in parallel to multiple instances of the "S&H circuit", the following is offered since such direct words were not used by *Pae*.

Examiner takes official notice that it was known to those skilled in the art to drive the control terminals of multiple transistors from a single controlled voltage source. As an example of awareness of this in the prior art, see for example Fig. 4 of the instant application in which transistor 2, responsive to a control signal I_{ref}, generates a controlled voltage that is supplied to three transistors in parallel.

Pae does not provide a drawing showing explicit partitioning and duplication of the elements of Fig. 3 and in particular does not show a drawing of a single "Vramp" signal connected to multiple "S&H circuit"s. The limits of the partitioning, however, are easily determined: at one extreme duplicating a given element once for the display and at the other extreme duplicating that element for every pixel. Given *Pae*'s notice that the "Vramp" signal was supplied from a circuit "external" to that shown in Fig. 3 and the knowledge that a voltage signal can be used to drive the gates of multiple transistors, the limits concerning the generators for "Vramp" are from one per display to one per "S&H circuit". At the time of the invention it would have been obvious to one of ordinary skill in the art to arrive at an implementation of *Pea* including the connection of a multiplicity of "S&H circuit"s, i.e. first switches to each "Vramp", i.e. controllable voltage source.

Thus *Pae* discloses or reasonably suggests to one of ordinary skill in the art the claimed invention except for the first switch being provided in each element and the use of a controllable voltage source in which a control electrode of a second current control means is connected to the control signal line such that the multiplicity of the first current control means and the second current control means form a correspond multiplicity of current mirror circuits connected in parallel when the respective first and second switching means are conducting.

Kimura discloses (Here examiner repeats citations for elements already taught in *Pea* in order to point out the fundamental similarity between the circuits disclosed in *Kimura* and *Pea*. For ease of reference, citations for the elements not taught in Pea are set off by a paragraph break below.) a display device and driving method for a multiplicity of elements arranged in rows and columns comprising a first switching means (see for example Fig. 44 item 1448) provided in each element which is controlled by a first switching signal (see for example Fig. 44 "dot-sequential line CLP"), and a second switching means (see for example Fig. 44 item 1444) which is arranged in series with the first switching means between a control signal line and the control electrode of a first current control means (see for example Fig. 44 item 112 "current supply transistor") and which is controlled by a second switching signal (see for example Fig. 44 "signal line GH") to store a current control voltage (see for example Fig. 44 "Vgs" of item 1445) that is generated by means of

a controllable voltage source comprising a second current control means (see for example Fig. 44 transistor 1445) in which a control electrode of the second current control means (see for example Fig. 44 transistor 1445) is connected to a control signal line (see for example Fig. 44 the line connecting to transistor 1448 to which the line connecting to the gate of transistor 1445 connects) such that the first current control means and the second current control means form a corresponding current mirror circuit when the respective first and second switching means of the multiplicity of elements are conducting (see for

example Fig. 44, note that current transistor 1445 is responsive to a control current supplied through current line CL and forms a current mirror circuit with current supply transistor 112).

Pae and *Kimura* are analogous art because they are from the same field of endeavor, which is active matrix displays.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to improve the circuit of *Pae* by using a controllable voltage source comprising a transistor connected in a current-mirror configuration as taught by *Kimura* as the controllable voltage source of *Pae*. The suggestion/motivation would have been to provide advantages such as to ensure that a constant current flows irrespective of fluctuation in threshold voltage, mobility, or the like (see for example Kimura 5:38-45) or to use an art recognized type of controllable voltage source or to use a type of controllable voltage source that inherently compensates for some noise and degradation factors (see for example *Kimura* 8:52-54 "same current characteristics").

At the time of invention, it would have been obvious to a person of ordinary skill in the art to improve the circuit of *Pae* by repeating the "S&H circuit" function of Pae in each element as taught by *Kimura*. The suggestion/motivation would have been to provide advantages such as to allow the current level to be set in a dot-sequential fashion (see for example 59:9-17) or to use a known alternative addressing circuit.

As to **claim 18**, in addition to the rejection of claim 17 over *Pae* and *Kimura*:

Pae further discloses a drive voltage signal cyclically falling from a predetermined starting value to an end value applied to a terminal of the switching means (see for example Fig. 2-4 "ramp").

Kimura further discloses the controllable voltage source controlled by a drive signal (see for example Fig. 44 "current line CL") switchably supplied to the second current control means via third switching means (see for example Fig. 44 item 1443), wherein the control signal supplied to the control electrode of the first current control means is dependent on the drive signal (see for example Fig. 44).

Pae and *Kimura* disclose the claimed invention except for the signal rising instead of falling. Since both rising and falling ramps were known to those skilled in the art and positive and negative voltage driven transistors were known it would have been obvious to one skilled in the art to replace a positive going ramp for a negative going ramp. One of ordinary skill could have implemented the modification and it would not have been beyond the reach of ordinary skill to consider both alternatives.

As to **claim 20**, in addition to the rejection of claim 17 over *Pae* and *Kimura*, both *Pae* and *Kimura* further disclose a signal holding means connected to the control electrode of the first current control means wherein the control signal is held when the first and/or second switching means interrupts the supply

of the control signal to the control electrode of the first current control means (see for example the capacitors of Pae Fig. 2 "Cs" and Kimura Fig. 44 item 111).

As to **claim 22**, in addition to the rejection of claim 17 over *Pae* and *Kimura*, *Kimura* further discloses a common first switching signal is supplied to a plurality of first switching means in elements in a line and/or a column (see for example Fig. 45).

Claim 23 claims the method implicit in the rejection of claim 18 plus the rejection of claim 17 and is rejected on the same grounds and arguments.

Claim 24 claims the method implicit in the rejection of claim 22 plus the rejection of claim 18 plus the rejection of claim 17 and is rejected on the same grounds and arguments.

As to **claim 26**, in addition to the rejection of claim 23 over *Pae* and *Kimura*, *Pae* further discloses an idle time provided between two cycles (see for example Fig. 4 period T2, which shows a flat or idle period in Vramp between the ramping cycles).

As to **claims 27, 28 and 29**, in addition to the rejection of claim 17 over *Pae* and *Kimura*:

Already disclosed in the rejection of claim 17 is the teaching that the current control means is a controllable voltage source applied from the control electrode and claims 27, 28 and 29 are rejected on the same grounds and arguments as claims 17, 20 and 22 respectively.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,992,647 to Hanada et al. discloses a multiplicity of first current control elements connected in parallel to a second current control element to produce a multiplicity of current mirrors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/RR/

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